WHAT IS CLAIMED IS:

1. A method for etching a capacitor structure within a silicon substrate, said method comprising:

providing a masked substrate comprising a patterned masking layer over said silicon substrate, said patterned masking layer having at least one aperture formed therein;

performing a series of at least two process steps upon said masked substrate, said series of at least two process steps comprising an isotropic plasma etching step in which said silicon substrate is etched through said at least one aperture; and

repeating said series of at least two process steps until a desired etch depth for said capacitor structure is achieved, wherein said capacitor structure has etched sidewall with a undulating profile.

2. The method according to claim 1 wherein said capacitor structure ranges from 1-10.0 microns in vertical dimension.

3. The method according to claim 1, wherein said capacitor structure is a trench.

4. The method according to claim 1 wherein said capacitor structure is an elevated structure.

5. The method according to claim 1 wherein said series of at least two process steps comprises (1) an isotropic plasma-etching step and (2) an anisotropic plasma-etching step.

6. The method according to claim 1 wherein said series of at least two steps comprises (1) an isotropic plasma etching step and (2) a plasma deposition step in which a passivating layer is deposited on said substrate.

7. The method according to claim 5 wherein said isotropic etching step is performed in the presence of a source gas comprising one or more of SF_6, Cl_2, NF_3 and CF_4,

8. The method according to claim 7 wherein said isotropic etching step is performed in the presence of a source gas comprising SF_6.

9. The method according to claim 5 wherein said anisotropic etching step is performed in the presence of a plasma source gas comprising SF_6 , HBr and O_2.

10. The method according to claim 9 wherein a SF_6 : HBr: O_2 ratio is about 1:1:1.

11. The method according to claim 6 wherein said isotropic etching step is performed in the presence of a source gas comprising one or more of SF_6, Cl_2, NF_3 and CF_4.

12. The method according to claim 6 wherein said isotropic etching step is performed in the presence of a source gas comprising SF_6.

13. The method according to claim 6, wherein said deposition step is performed in the presence of a fluorocarbon gas or a fluorohydrocarbon gas.

14. The method according to claim 6, wherein said deposition step is performed in the presence of one or more of C_4F_8, CH_2F_2, CHF_3, and C_4F_6.

15. The method according to claim 6, wherein said deposition step is performed in the presence of C_4F_8.

16. The method according to claim 1 wherein said etching step is conducted at a plasma density ranging from 10^{11} to 10^{12} cm^{-3}.

17. The method according to claim 1 wherein said etching step proceeds at a rate ranging from 1-3 microns per minute.

18. A capacitor structure formed by a process comprising:

providing a masked substrate comprising a patterned masking layer over said silicon substrate, said patterned masking layer having at least one aperture formed therein;

performing a series of at least two process steps upon said masked substrate, said series of at least two process steps comprising an isotropic plasma etching step in which said silicon substrate is etched through said at least one aperture; and

repeating said series of at least two process steps until a desired etch depth for said capacitor structure is achieved, wherein said capacitor structure has etched sidewall with a undulating profile.

19. The capacitor structure according to claim 18, wherein said capacitor structure ranges from 1-10.0 microns in vertical dimension.

20. The capacitor structure according to claim 18, wherein said capacitor structure is a trench.

21. The capacitor structure according to claim 18, wherein said capacitor structure is one of a portion of a stacked capacitor and a trench capacitor.

22. The capacitor structure according to claim 18, wherein said series of at least two process steps comprises (1) an anisotropic plasma-etching step and (2) an isotropic plasma-etching step.

23. The capacitor structure according to claim 18 wherein said series of at least two process steps comprises (1) an isotropic plasma etching step and (2) a plasma deposition step in which a passivating layer is deposed on said substrate.